Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 8, 10-13, and 16-22 are pending in the application, with claims 8 and 18 being the independent claims. Claims 8 and 10-13 are sought to be amended. Applicants reserve the right to prosecute similar or broader claims, with respect to the amended claims, in the future. New claims 16-22 are sought to be added. These changes are believed to introduce no new matter, and their entry is respectfully requested.

With respect to this Application, Applicants hereby rescind any disclaimer of claim scope made in the parent application or any predecessor or related application. The Examiner is advised that any previous disclaimer of claim scope, if any, and the alleged references that it was made to allegedly avoid, may need to be revisited. Nor should any previous disclaimer of claim scope, if any, in this Application be read back into any predecessor or related application.

Based on the above amendment and the following remarks, Applicant respectfully requests that the Examiner reconsider all outstanding rejections and that they be withdrawn.

Rejections under 35 U.S.C. § 102

Claims 8-10, 12, and 13

Claims 8-10, 12, and 13 stand rejected under 35 U.S.C. § 102(a) as allegedly being anticipated by United States Patent No. 6,598,191 to Sharma et al. (herein

"Sharma"). Applicants respectfully traverse the rejection and provide the following arguments to support patentability.

For a rejection to be sufficient under 35 U.S.C. § 102, ***every claim limitation must be taught in a single reference.*** Industries, Inc. v. Guardian Industries Corp., 75 F.3d 1558, 1566 (Fed. Cir. 1996) (emphasis added). The absence of any claimed element from the reference negates anticipation. Atlas Powder Co. v. E.I. du Pont de Nemours & Co., 750 F.2d 1569, 1574 (Fed. Cir. 1984). As will be described in more detail below, Sharma does not teach or suggest at least the features of "a second asynchronous clock domain, coupled to the first asynchronous clock domain, including one or more jitter elements, wherein at least one of the one or more jitter elements is insertable in the second asynchronous clock domain at a circuit boundary between the first asynchronous clock domain and the second asynchronous clock domain" as recited by claim 8. Consequently, Sharma cannot anticipate amended claim 8.

Sharma

Sharma discloses an apparatus "for verifying the asynchronous boundary behavior of a digital system...where the asynchronous boundary is formed between two or more clock domains in the digital system." Sharma, col. 1, lines 6-10. One embodiment of Sharma, as disclosed in FIG. 7, includes "a model 132 having a separately clocked write domain 32 and a separately clocked read domain 34, wherein additional logic has been inserted in read domain 34 to allow proper verification of the asynchronous boundary behavior between the domains." Sharma, col. 11, lines 44-49. An asynchronous boundary 36 is formed between the clocked write domain 32 and the read domain 34. *See*, Sharma, col. 5, lines 44-45. The additional logic of Sharma

includes "extend flip flops 104, 106, and 108 and multiplexers 110, 112, and 114 in read domain 34 rather than write domain 32." Sharma, col. 11, lines 56-58. As shown in FIG. 7 of Sharma, the write domain 32 includes first level read flip flops 52, 54, and, 56 and the read domain 34 includes first level read flip flops 52, 54, and 56. According to Sharma,

> the outputs of write flip flops 44, 46, and 48 are coupled to corresponding inputs of first level read flip flops 52, 54, and 56 via signal... The outputs of first level read flip flops 52, 54, and 56 are coupled to the inputs of extend flip flops 104, 106, and 108... The outputs of first level read flip flops 52, 54, and 56 are also coupled to the inputs of multiplexers 110, 112, and 114... The outputs of extend flip flops are connected to corresponding inputs of multiplexers 110, 112, and 114...
>
> Sharma, col. 11, line 58 through col. 12, line 3.

However, as shown in FIG. 7 of Sharma, the asynchronous boundary 36 of Sharma is positioned in between the write flip flops 44, 46, and 48 and the first level read flip flops 52, 54, and 56. As a result, Sharma does not teach or suggest inserting the extend flip flops 104, 106, and 108 and multiplexers 110, 112, and 114 in the read domain 34 ***at a circuit boundary*** between the write domain 32 and the read domain 34 as recited by claim 8. As a result, Sharma does not teach or suggest at least the feature of "a second asynchronous clock domain, coupled to the first asynchronous clock domain, including one or more jitter elements, wherein at least one of the one or more jitter elements is insertable in the second asynchronous clock domain at a circuit boundary between the first asynchronous clock domain and the second asynchronous clock domain" as recited by claim 8. Dependent claims 10, 12, and 13 are likewise not anticipated by Sharma for the same reasons as discussed above and further in view of their own respective features.

Accordingly, Applicants respectfully requests that the rejection of claims 8, 10, 12, and 13 under 35 U.S.C. § 102(a) be reconsidered and withdrawn.

Rejections under 35 U.S.C. § 103

Claims 8 and 11-13

Claims 8 and 11-13 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over United States Patent Publication No. 2003/0125916 to Benis (herein "Benis"). Applicants respectfully traverse the rejection and provide the following arguments to support patentability.

Benis discloses a "method for simulating and synthesizing an array of flip-flops, including metastable effects." Benis, para. [0001]. To "simulate the array of flip flops and in particular to model metastable effects, three registers 480, 482 and 484 are defined for simulation of the circuit only (that is, these registers are not used for synthesis of the circuit)." Benis, para. [0035]. Benis further provides:

> the simulation of the array with metastable effects also includes a simulated multiplexer (MUX) 460 that receives inputs from registers 480 and 482, multiplexes those inputs, and provides outputs to register 484. In this embodiment, MUX 460 multiplexes the inputs from registers 480 and 482 responsive to [a random number generator 470].
>
> Benis, para. [0036].

Assuming *arguendo* that the three registers 480, 482, and 484, the simulated multiplexer 460, and the random number generator 470 comprise "jitter elements," Benis is silent regarding the location of these aforementioned elements relative to the asynchronous clock domains as previously argued in an Amendment and Reply Under 37 C.F.R. §

1.111 as filed on August 29, 2008 (herein "Amendment and Reply"). *See*, Amendment and Reply, Page 11.

In response, the "Examiner notes the simulated metastable boundary is between the first rank and second rank of flip flops where the metastable boundary indicates the boundary between the asynchronous clock domains." Office Action dated December 5, 2008 (herein "Office Action"), Page 4. According to the Office Action,

> [i]f one is to extend the metastable boundary line down to the multiplexer's left side ...incident with the metastable boundary indicating that the multiplexer is in the second clock domain...
>
> Office Action, Page 4.

However, the Examiner cannot simply extend the metastable boundary line down to the multiplexer. There is no teaching or suggestion in Benis that the boundary line may be extended down to the multiplexer. Extending the boundary line down to the multiplexer is not capable of "instant and unquestionable demonstration as being well-known" and thus are not appropriate subject matter for the taking of Official Notice. *See*, In re Zurko, 258 F.3d 1379, 1385 (Fed. Cir. 2001)(holding that general conclusions concerning what is "basic knowledge" or "common sense" to one of ordinary skill in the art without specific factual findings and some concrete evidence in the record to support these findings will not support an obviousness rejection); *see also*, generally, M.P.E.P. § 2144.03. For example, Benis at most teaches that the metastable boundary line may occur between "any two ranks of flip flops." Benis, para. [0033]. Accordingly, Benis does not teach or suggest at least the feature of "a second asynchronous clock domain, coupled to the first asynchronous clock domain, including one or more jitter elements, wherein at least one of the one or more jitter elements is insertable in the second

asynchronous clock domain at a circuit boundary between the first asynchronous clock domain and the second asynchronous clock domain" as recited by claim 8. Consequently, Benis does not render claim 8 obvious. Dependent claims 11- 13 are likewise not rendered obvious by Sharma for the same reasons as discussed above and further in view of their own respective features. Accordingly, Applicants respectfully requests that the rejection of claims 8 and 11-13 under 35 U.S.C. § 103(a) be reconsidered and withdrawn.

New claims

New claims 16-22 have been added. From the discussion above, Applicants have traversed the rejections to independent claim 8. Dependent claims 16 and 17 are likewise allowable for the same reasons as the independent claim from which they respectively depend and further in view of their own respective features.

For reasons discussed above in regard to claim 8, Applicants respectfully submit that claim 16 is patentable over the art of record. For example, Sharma and/or Benis does not to teach or suggest at least the feature of "wherein at least one of the one or more jitter elements is insertable in the second asynchronous clock domain at a circuit boundary between the first asynchronous clock domain and the second asynchronous clock domain" as recited by claim 18. Dependent claims 19-22 are also patentable over the art of record for the same reason as claim 18 from which they depend and further in view of their own respective features.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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